AMENDMENTS TO THE CLAIMS

Please add new claims 44-49 as indicated below.

Listing of the Claim:

Claims 1-41: (Cancelled.)

42.(Previously Presented) A non-volatile semiconductor memory device, comprising:

a memory array including a plurality of multi-level-cell memory cells, each memory cell comprising a storage element having a capacity to store N bits of logical data,

where $N \geq 2$, and each memory cell configured for 2^N distinct data storage levels, each of the 2^N data storage levels representative of a discrete N-bit combination of logical data; and

a staircase program-verify circuit for providing a staircase program-verify pulse electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells and inhibiting programming of a memory cell programmed to substantially within a selected data storage level.

43.(Previously Presented) The device of claim 42, wherein the storage element comprises a semiconductor transistor having a programmable threshold voltage, V_t, within a continuous range from a lowest V_t value to a highest V_t value, the continuous range having 2^N distinct data storage levels including an erased level and 2^N-1 program levels, the 2^N-1 program levels including a lowest program level, at least one intermediate program level, and a highest program level.

44.(New) The device of claim 42, wherein the staircase program-verify pulse is a staircase of composed of steps of increasing current level.

45.(New) The device of claim 42, wherein the staircase program-verify pulse is a staircase of composed of steps of increasing voltage level.

46.(New) The device of claim 42, further comprising:

a staircase read/sense circuit for providing a staircase read pulse electrically coupled to the memory array and capable of concurrently reading the plurality of multi-level-cell memory cells, wherein the staircase read pulse is formed of steps of a higher level of resolution than the program-verify pulse.

47.(New) A non-volatile semiconductor memory device, comprising:

a memory array including a plurality of multi-level-cell memory cells, each memory cell comprising a storage element having a capacity to store N bits of logical data,

where $N \geq 2$, and each memory cell configured for 2^N distinct data storage levels, each of the 2^N data storage levels representative of a discrete N-bit combination of logical data;

a plurality of current sources providing a respective plurality of current levels each corresponding one of the distinct storage levels; and

a program-verify circuit coupled to receive said plurality of current sources and electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells individually against the current level corresponding the cell's selected data storage level and inhibiting programming of a memory cell programmed to substantially within the corresponding selected data storage level.

48.(New) The device of claim 47, wherein the number of current levels is 2^N-1.

49.(New) The device of claim 47, further comprising:

a data-in register to store the selected data storage level for each of the plurality of multi-level-cell memory cells according to which the corresponding current level is selected for program-verifying.